CLAIMS

What is claimed is:

1. A digital signal processing system, comprising:

at least one shared component;

a plurality of processor subsystems that share said shared component; and

a clock tree configured to provide a clock signal to said shared component, wherein the clock signal is disabled only if each of the plurality of processor subsystems disables the shared component.

2. The system of claim 1, wherein the plurality of processor subsystems, the shared component, and the clock tree are fabricated on a single chip.

3. The system of claim 1, wherein the shared component comprises a shared program memory.

4. The system of claim 1, wherein the shared component comprises an external input/output port (XPORT) arbiter.

5. The system of claim 4, wherein each of the plurality of processor subsystems includes a processor core having an external input/output port (XPORT) interface coupled to an external input/output port (XPORT).

6. The system of claim 5, wherein the clock tree supplies a corresponding processor clock signal to each of the processor cores, and wherein the clock tree is configured to separately and independently disable the processor cores by suspension of the corresponding processor clock signal from the clock tree.

7. The system of claim 6, wherein the processor clock signals are distinct from the clock signal to the shared component, and wherein the XPORT interfaces each receive the clock signal to the shared component.

8. The system of claim 7, wherein the XPORT arbiter is coupled to each of the XPORT interfaces and is configured to assert a hold signal to the XPORT interfaces when another component requests access to the XPORT, wherein the XPORT arbiter requires an assertion of a hold acknowledge signal from each of the XPORT interfaces before granting the requested XPORT access.

9. The system of claim 1, wherein the clock tree includes a register having a plurality of enablement bits, each of said enablement bits configured to enable a corresponding one of a plurality of clock signals when asserted, wherein said plurality of clock signals are coupled to a corresponding plurality of processor subsystems.

10. The system of claim 9, wherein the clock tree further includes a clock gate for each of the plurality of clock signals, wherein said each clock gate is at least one of said plurality of enablement bits from said register.

11. The system of claim 10, wherein the clock tree further includes a logic gate coupled to each of the shared component enablement bits and to one of said clock gates, wherein the logic gate is configured to assert a gate signal to said one of said clock gates for the shared component clock if at least one shared component enablement bit is asserted.

12. The system of claim 11, wherein said clock gates each comprise gated inverting buffers, and said logic gates comprise logical OR gates.

13. The system of claim 11, wherein said logic gates de-assert the gate signal to the corresponding clock gate if none of the shared component enablement bits are asserted.

14. A method of providing a clock signal to a shared component shared by a plurality of subsystems, wherein the method comprises:

generating a clock signal; and

passing the clock signal to the shared component only if at least one of the subsystems has not de-asserted a shared component enablement bit.

15. The method of claim 14, further comprising:

blocking the clock signal to the shared component only if each of the plurality of subsystems has de-asserted a corresponding shared component enablement bit.

16. The method of claim 14, wherein the plurality of subsystems and the shared component are fabricated on a single chip.

17. The method of claim 14, wherein the shared component comprises a shared program memory.

18. The method of claim 14, wherein the shared component comprises an external input/output port arbiter.

19. A digital signal processing chip that comprises:

an external input/output port (XPORT);

an external input/output port (XPORT) arbiter;

a plurality of processor cores configured to access the XPORT, wherein each of the plurality of processor cores includes an XPORT interface coupled to the XPORT arbiter; and

a clock tree configured to provide a clock signal to the XPORT arbiter and the XPORT interfaces, wherein the clock tree is configured to disable the clock signal if each of the plurality of processor cores de-asserts a respective peripheral enablement bit.

20. The chip of claim 19, wherein the clock tree includes a register having said respective enablement bits, wherein the clock tree further includes a logic gate coupled to each of the respective enablement bits and configured to assert a gate signal only if at least one shared component enablement bit is asserted.

21. The chip of claim 20, wherein the clock tree further includes a clock gate coupled to the logic gate to receive the gate signal, wherein the logic gate is configured to block the clock signal only if the gate signal is de-asserted.

22. The chip of claim 19, wherein the clock tree further provides processor clock signals distinct from the clock signal to the XPORT arbiter that are configured to be independently blocked and passed.